S, HOOD (PAL)

APPLICATION		REVISIONS			
NEXT ASSY.	USED ON	LTR	DESCRIPTION	DATE	APPROVED
	A500	A	PRODUCTION RELEASE	11-10-87	J Shorty
		B	REVISED PER ECO 880077	6-29-88	R. Buchs
		C	REVISED PER ECO 880093	7-20-88	R. Buchs

1.0 DESCRIPTION

This specification describes the requirements for an N-Channel HMOS DMA Controller. The IC device described herein shall produce, in a 68000 microprocessor environment, DMA addresses using a RAM Address Generator and a Register Address Encoder. This device shall contain 25 DMA channel controllers that include the Blitter, Bitplane, Copper, Audio, Sprites, Disk and Memory Refresh.

The IC shall accept a 28.375 MHz crystal clock for the purpose of generating 7.16 MHz and 3.55 MHz system clocks, dynamic RAM interface for addressing up to one (1) megabyte of memory and PAL video synchronization pulses.

Refer to Figure 1 for Pin Configuration, Figure 2 for IC Block Diagram and Table 1 for Pin Description. This IC device shall be equivalent to an 8371.
Refer to Table 2 for Register Addresses.

1.1 CONFIGURATION

This IC device shall be configured in a standard, 84-pin plastic chip carrier package.

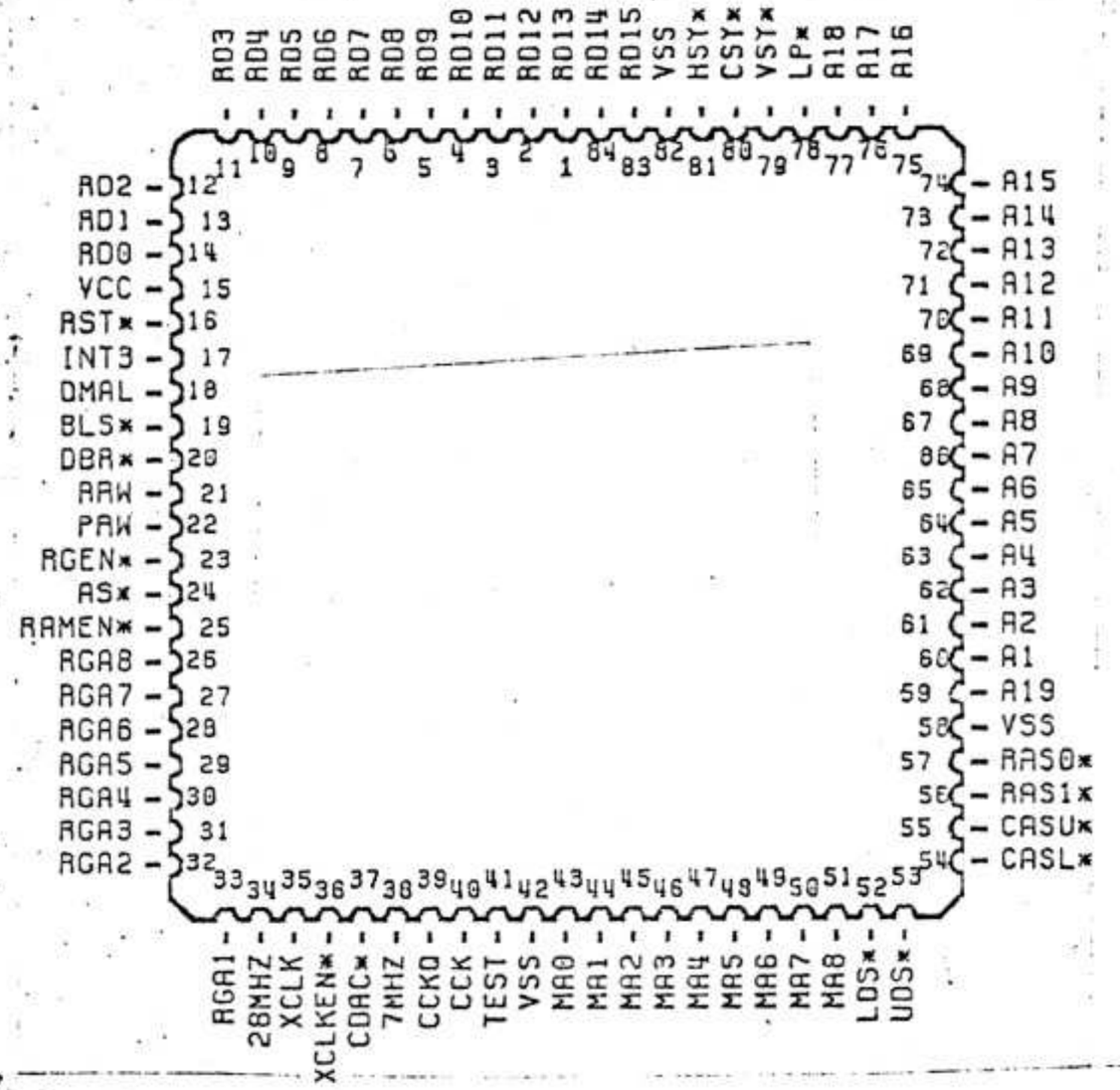

FIGURE 1

CONFIGURATION

COMMODORE PART #	STATUS
318071-01	Active

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

TOLERANCES
ANGLES +/- 1 DEGREE
2 PLACE DECIMALS +/-.02
3 PLACE DECIMALS +/- .010

DRWN	J.F.Broderick	1-28-87
SYSTEMS ENG		
TEST ENG		4/15/87
CIRCUIT ENG	L. F. Broderick	4/15/87
COMP ENG	R. T. Buchs	3/20/87

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TITLE IC, N-CHANNEL-HMOS DMA CONTROLLER (PAL) "FAT AGNUS" 8371

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FIGURE 2 - BLOCK DIAGRAM

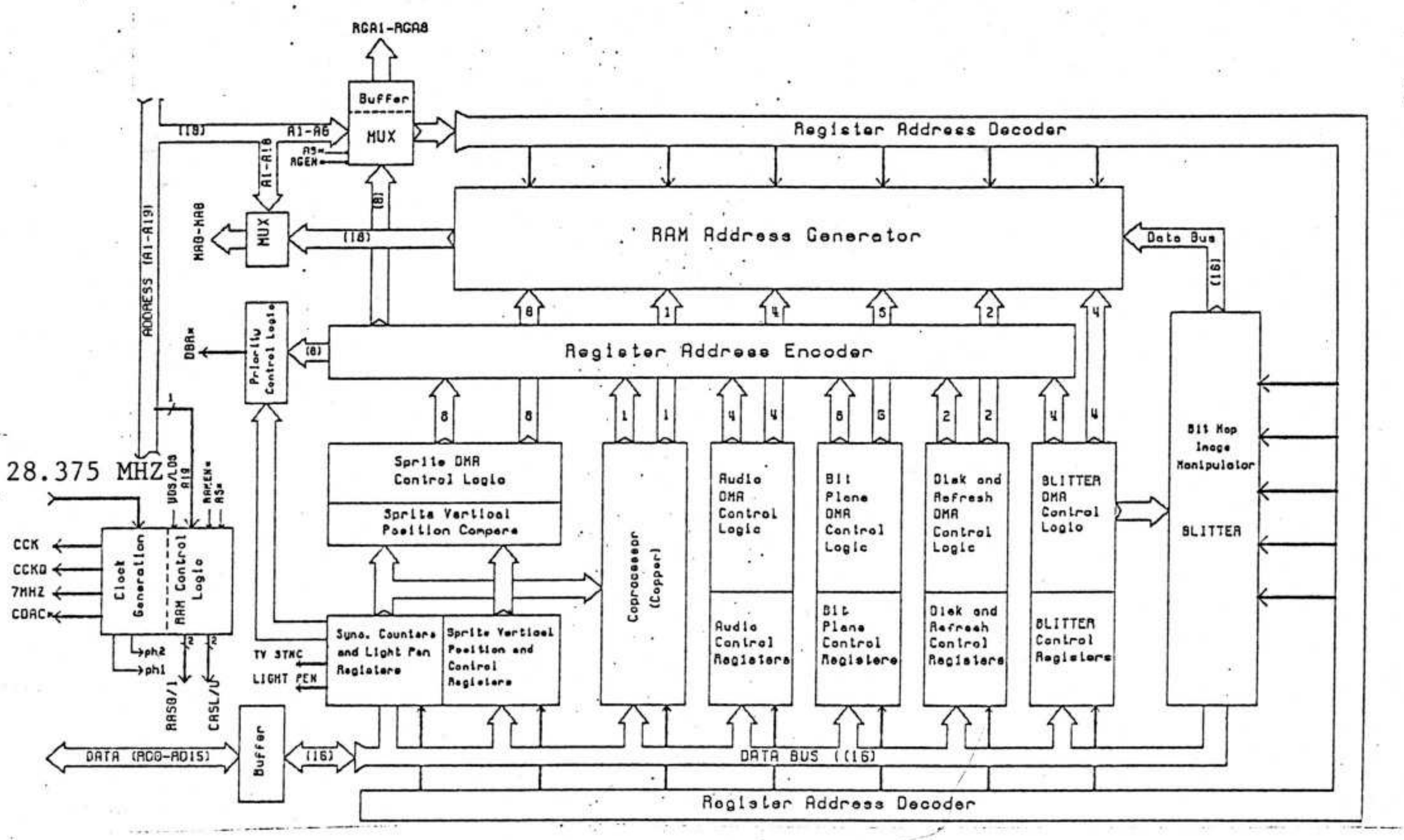

TABLE 1 - PIN DESCRIPTION

PIN NAME	PIN NUMBER	SIGNAL DIRECTION	DESCRIPTION
A19-A1	59 thru 77	IN	Address bus - A1 to A8 are used by the processor to select the internal registers and put an address code on the RGA lines to select registers outside the device. The processor uses A1 to A18 to generate multiplexed DRAM addresses on the MA outputs. The A19 line is used to indicate which RAS line is activated. If A19 is high RAS1* is asserted; if low, RAS0* is asserted.
RD15-RD0	1 thru 14 and 83 & 84	I/O	This data bus is buffered and is used by the processor to access the device registers. The data bus is also accessed during DMA operations.

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TABLE 1 - PIN DESCRIPTION (CONT'D)

PIN NAME	PIN NUMBER	SIGNAL DIRECTION	DESCRIPTION
AS*	24	IN	Active low. This input is the processor address strobe signal. When asserted, it indicates that the address lines (A1 to A19) are valid.
RGEN*	23	IN	Active low. When this signal is asserted along with AS*, the processor uses A1 to A8 to access one of the device registers or put a value on the RGA outputs to select registers outside the device.
RAMEN*	25	IN	Active low. When this signal is asserted together with AS*, the processor is doing a DRAM access. The processer supplies an address on the A1 to A18 inputs and the device multiplexes this address onto the MA outputs; during the same cycle, the processor controls the A19 line to select one of the RAS lines.
PRW	22	IN	This signal defines the data bus transfer as a read or write cycle to memory. The signal is only enabled when the processor is undergoing a DRAM access. A low on this signal signifies a processor write cycle to memory; a high indicates a processor read cycle from memory.
RRW	21	OUT	The device controls this signal to indicate either a DMA or processor DRAM read/write access. In both cases, a low on this line indicates a write operation and a high indicates a read operation.
MA0-MA8	43 thru 51	OUT	Output bus. This 9 bit output bus provides multiplexed addresses to DRAMs. This bus operates in two cycles. The first cycle provides the DRAMs with the row address; the second cycle with the column address. It includes full 256K addressing for use with 256KX1 DRAMS. The IC only activates this bus when the processor is doing a DRAM access (RAMEN* is low) or when the device itself is performing a DMA data transfer (DBR* is low).

TABLE 1 - PIN DESCRIPTION (CONT'D)

PIN NAME	PIN NUMBER	SIGNAL DIRECTION	DESCRIPTION
LDS*	52	IN	Active low. This input is the processor lower data strobe. It is enabled only during a processor DRAM access and forces the IC to assert CASL* to select the lower 256K memory bank.
UDS*	53	IN	Active low. This input is the processor upper data strobe. It is enabled only during a processor DRAM access and forces the IC to assert CASU*to select the upper 256K memory bank.
CASL*	54	OUT	Active low. This output strobes the column address into the DRAMs and corresponds to the low byte of the data word.
CASU*	55	OUT	Active low. This output strobes the column address into the DRAMs and corresponds to the high byte of the data word.
RAS0*	57	OUT	Active low. This output is used to strobe the row address into the DRAMs. This signal will be asserted only if the processor is doing a DRAM access and A19 is low or if the IC is performing a DMA cycle (DBR* is low). RAS0* corresponds to the lower 512K bytes of memory.
RAS1*	56	OUT	Active low. This output is used to strobe the row address into the DRAMs. This signal will be asserted only if the processor is doing a DRAM access and A19 is high. The signal will not be asserted when the device is doing a DMA cycle. RAS1* corresponds to the upper 512K bytes of memory.
DBR*	20	OUT	Active low. The device asserts this signal to indicate that a DMA cycle is underway. The device performs DMAs only on the lower 512K bytes of memory when DBR* is low and RAS0* is asserted. The only exception is when the device performs a DRAM refresh, in which case RAS0*, RAS1* and DBR* are all asserted. The device will also assert both CASL* and CASU* during DMAs except on a DRAM refresh cycle.

TABLE 1 - PIN DESCRIPTION (CONT'D)

PIN NAME	PIN NUMBER	SIGNAL DIRECTION	DESCRIPTION
RGA8-RGA1	26 thru 33	OUT	Output bus. The 8 bit output bus allows the device and the processor to access registers located outside the device.
HSY*	81	I/O	This line is bidirectional and buffered. This signal is the horizontal synchronization pulse and is PAL compatible. When set as an input, an external video source drives this signal to synchronize the horizontal beam counter.
VSY*	79	I/O	This line is bidirectional and buffered. This signal is the vertical synchronization pulse and is PAL compatible.When set as an input, an external video source drives this signal to synchronize the vertical beam counter.
CSY*	80	OUT	This signal is the composite video synchronization pulse and is PAL compatible.
LP*	78	IN	Active low. This input is used to indicate when the light pen is coincident with the monitor beam.
RST*	18	IN	Active low. This input will initialize the device to a known state.
INT3*	17	OUT	Active low. The device asserts this line to indicate that the blitter has completed the requested data transfer and that the blitter is then ready to accept another task.
DMAL	18	IN	Active high. When this signal is enabled, it indicates that an external device is requesting audio and/or disk DMA cycles to be executed by the device.
BLS*	19	IN	Active low. When this line is asserted, the device will suspend its blitter operation and allows the processer to have control of the cycle.
28MHZ	34	IN	This is a 28.375MHz input clock that provides the master time base for the device. This clock is enabled only when XCLKEN* is high.

TABLE 1 - PIN DESCRIPTION (CONT'D)

PIN NAME	PIN NUMBER	SIGNAL DIRECTION	DESCRIPTION
XCLK	35	IN	This input is an alternate master clock to the device. It is enabled when XCLKEN* is low. This input is used to synchronize the device with an external video source.
XCLKEN*	36	IN	This input is used to select the master clock to the device. If it is high, the 28MHz input is enabled; if low, the XCLK is enabled.
CCK	40	OUT	This signal is a clock, which is obtained after dividing the 28.375MHz clock by eight.
CCKQ	39	OUT	This clock is the CCK clock shifted by 90 degrees.
7MHZ	38	OUT	This clock is obtained after dividing the 28MHZ clock by four.
CDAC*	37	OUT	This clock is obtained after inverting the 7MHZ clock and shifting it by 90 degrees.
TEST	41	IN	Active high. When this signal is asserted it disables the processor cycle and the 8371 internal registers can be accessed on every CCK clock cycle.

1.2 SOURCES

Refer to the Approved Vendors List for approved sources.

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DMA CONTROLLER (PAL)
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2.0 ELECTRICAL PARAMETERS

2.1 ABSOLUTE MAXIMUM RATINGS

Stress above those listed may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

CHARACTERISTIC		MIN	MAX	UNITS
2.1.1	Ambient Temperature under Bias	-25°	+125°	C
2.1.2	Storage Temperature	-65°	+150°	C
2.1.3	Applied Supply Voltage	-0.5	+7.0	V
2.1.4	Applied Output Voltage	-0.5	+5.5	V
2.1.5	Applied Input Voltage	-2.0	+7.0	V
2.1.6	Power Dissipation	-	1.5	W

2.2 OPERATING CONDITIONS

All electrical characteristics are specified over the entire range of operating conditions, unless specifically noted. All voltages are referenced to V_{SS} = 0.0V.

CONDITION		MIN	MAX	UNITS
2.2.1	Supply Voltage (V_{CC})	4.75	5.25	V
2.2.2	Free Air Temperature	0	70	°C

2.3 D.C. CHARACTERISTICS

CHARACTERISTIC		SYMBOL	MIN	MAX	UNITS	CONDITIONS
2.3.1	Input High Level	Vih	2.0	V_{CC}+1	V	-
2.3.2	Input Low Level	Vil	-0.5	+0.8	V	-
2.3.3	Output High Level	Voh	+2.4	-	V	Ioh=300uA
2.3.4	Output Low Level	Vol	-	0.4	V	Iol=4.8mA
2.3.5	Input Leakage	Iin	-10	+10	uA	0.0V<Vin<Vcc
2.3.6	Output Leakage	Ilkg	-10	20	uA	.4V<Vout<2.4V
2.3.7	Supply Current	Icc	-	200	mA	Outputs open
2.3.8	Capacitance	Cpin	-	10	pF	-

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2.0 ELECTRICAL PARAMETERS (CONT'D)

2.4 A.C. CHARACTERISTICS

Refer to Figure thru for waveform diagrams.

CLOCK RELATIONS (Refer to Figure 4)

		SYMBOL	MIN	MAX	UNIT
2.4.1	28MHz clock cycle	t28MC	34.57	35.27	ns
2.4.2	28MHz clock high	t28MHi	12.0	22.9	ns
2.4.3	28MHz clock low	t28MLo	12.0	22.9	ns
2.4.4	CCK clock cycle	tcyc	260	290	ns
2.4.5	CCK clock high	tch	130	150	ns
2.4.6	CCK clock low	tcl	130	150	ns
2.4.7	CCK-CCKQ clock separation	tcq	65	75	ns
2.4.8	7MHz clock cycle	t7MC	130	150	ns
2.4.9	7MHz clock high	t7MHi	65	75	ns
2.4.10	7MHz clock low	t7MLo	65	75	ns
2.4.11	7MHz-CDACQ clock separation	t7MQ	30	40	ns
2.4.12	CCK to 7MHz delay	tc7M	0	15	ns
2.4.13	CCKQ to 7MHz delay	tQ7M	0	15	ns
2.4.14	Clock rise time	tr	0	10	ns
2.4.15	Clock fall time	tf	0	10	ns

PROCESSOR ACCESS (Refer to Figure 5)

		SYMBOL	MIN	MAX	UNIT
2.4.16	Address input setup time	tAddins	45	-	ns
2.4.17	Address input hold time	taddinh	30	260	ns
2.4.18	Processor access control setup time	taccs	10	-	ns
2.4.19	Processor access control hold time	tacch	0	220	ns
2.4.20	Access to address invalid delay	taccad	30	-	ns
2.4.21	Processor CAS access setup time	tpcs	10	-	ns
2.4.22	Processor CAS access hold time	tpch	10	270	ns
2.4.23	Data input setup time	tdins	50	-	ns
2.4.24	Data input hold time	tdinh	0	-	ns
2.4.25	Reset input setup time	tresch	50	-	ns
2.4.26	Reset input hold time	tchresh	50	-	ns
2.4.27	Data Strobe Pulse Width	t_{DS}	115	-	ns
2.4.28	Write Pulse Width	t_{WP}	45	-	ns

2.0 ELECTRICAL PARAMETERS (CONT'D.)

2.4 A.C. CHARACTERISTICS (Cont'd.)

DEVICE ACCESS (Refer to Figure 5)

		SYMBOL	MIN	MAX	UNIT
2.4.27	CCK low to DBR valid prop time	tcldbr	0	120	ns
2.4.28	CCKQ high to RAS low prop time	tcqrl	7	18	ns
2.4.29	CCKQ low to RAS high prop time	tcqrh	28	38	ns
2.4.30	RAS precharge time prop time	trp	100	105	ns
2.4.31	CCK low to CAS low prop time	tckcl	-	6	ns
2.4.32	CCK high to CAS high prop time	tckch	-	6	ns
2.4.33	RAS address setup time	trass	0	-	ns
2.4.34	RAS address hold time	trash	15	-	ns
2.4.35	CAS address setup time	tcass	0	-	ns
2.4.36	CAS address hold time	tcash	25	-	ns
2.4.37	CCKQ low to RGA valid prop time	tqlrgao	-	110	ns
2.4.38	CCK low to RGA invalid prop time	tclrgaoh	10	-	ns
2.4.39	CCKQ high to Data valid prop time	tqhdo	0	150	ns
2.4.40	CCK high to Data invalid prop time	tchdoh	0	85	ns
2.4.41	CCK high to Early read Data prop time	tchedo	0	125	ns
2.4.42	Write command setup time	twcs	0	-	ns
2.4.43	Write command hold time	twch	45	-	ns

MISCELLANEOUS (Refer to Figure 6)

		SYMBOL	MIN	MAX	UNIT
2.4.44	LP*, DMAL input setup time	tiasch	50	-	ns
2.4.45	LP* input hold time	tchiah	50	-	ns
2.4.46	DMAL input hold time	tchdmalh	15	-	ns
2.4.47	BLS* input setup time	tiascl	50	-	ns
2.4.48	BLS* input hold time	tcliah	50	-	ns
2.4.49	VSY*, INT3* output prop time	tchob	10	110	ns
2.4.50	CSY*, HSY* output prop time	tcob	0	110	ns
2.4.51	VSY*, HSY* input setup time	tibsch	30	-	ns
2.4.52	VSY*, HSY* input hold time	tchibh	30	-	ns

FIGURE 3

CLOCK RELATIONS

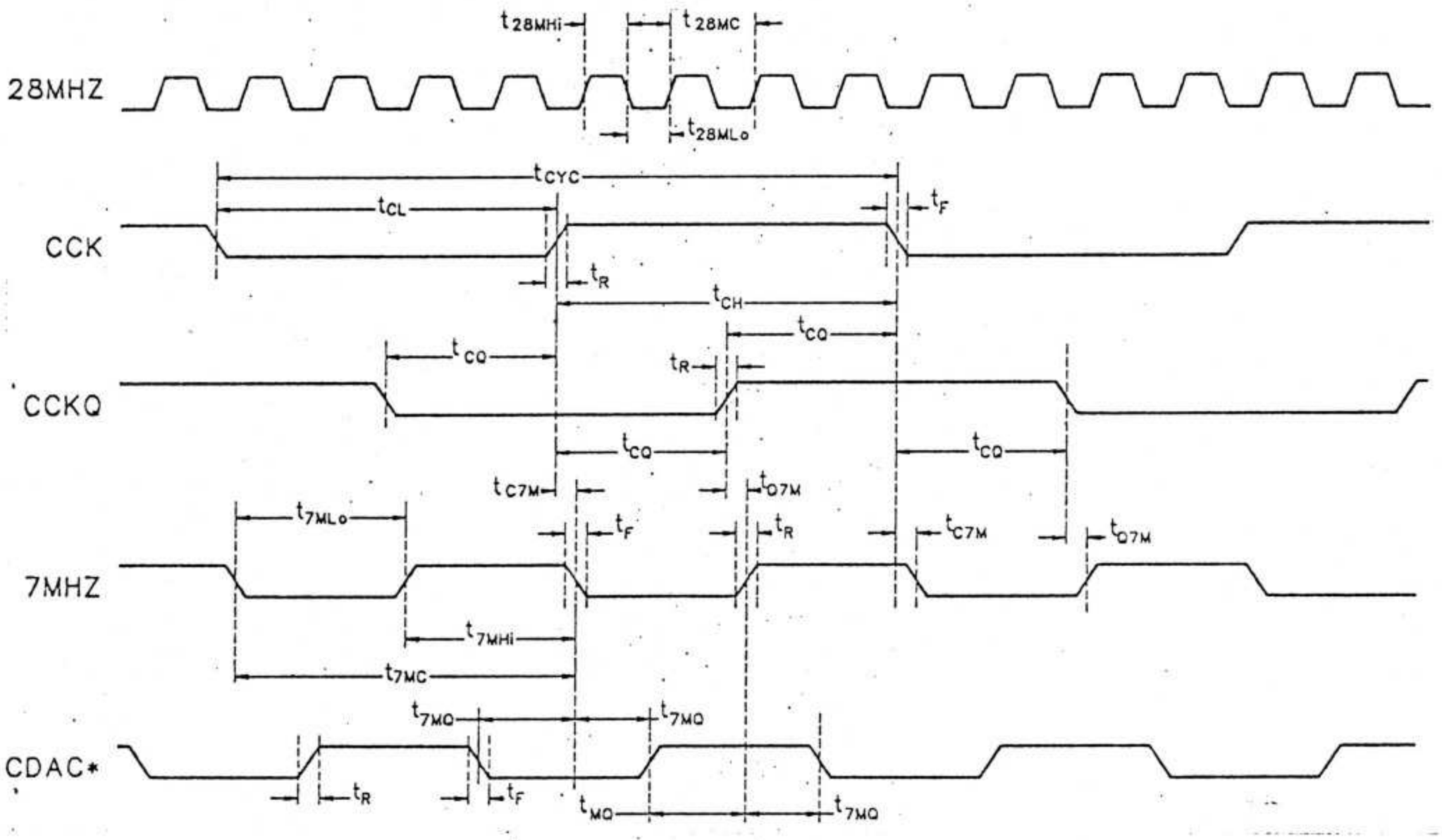

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FIGURE 4

PROCESSOR ACCESS

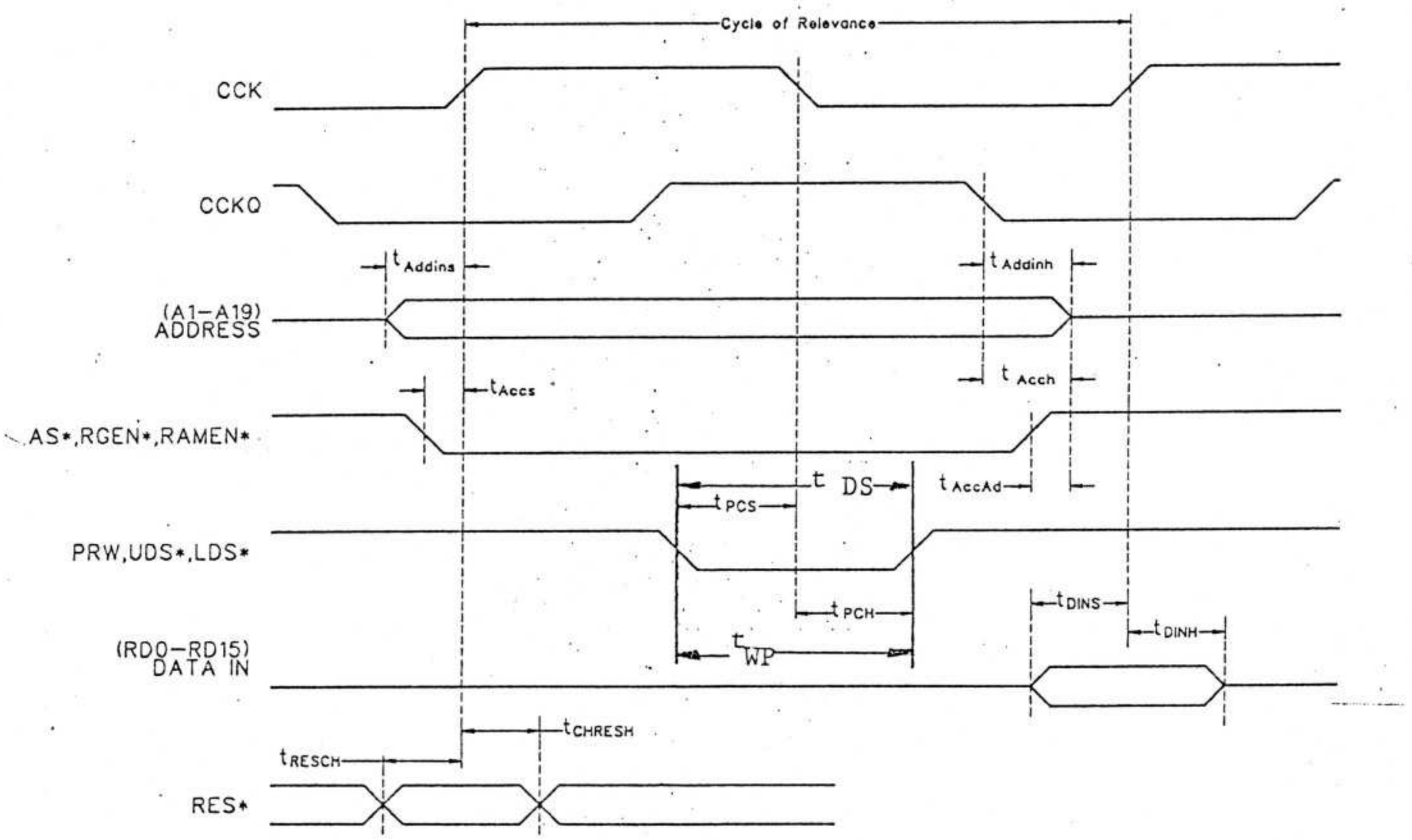

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FIGURE 5

DEVICE ACCESS

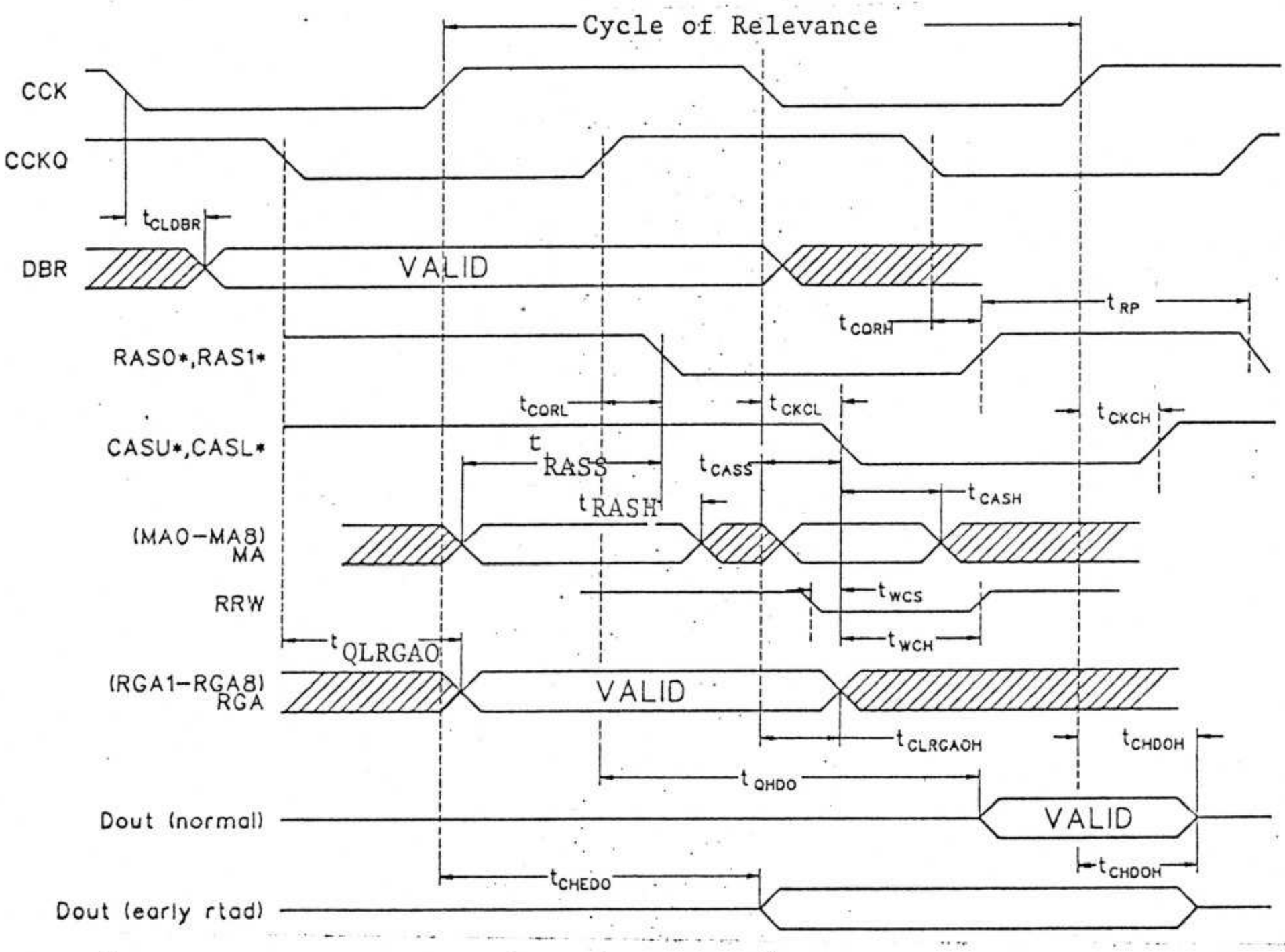

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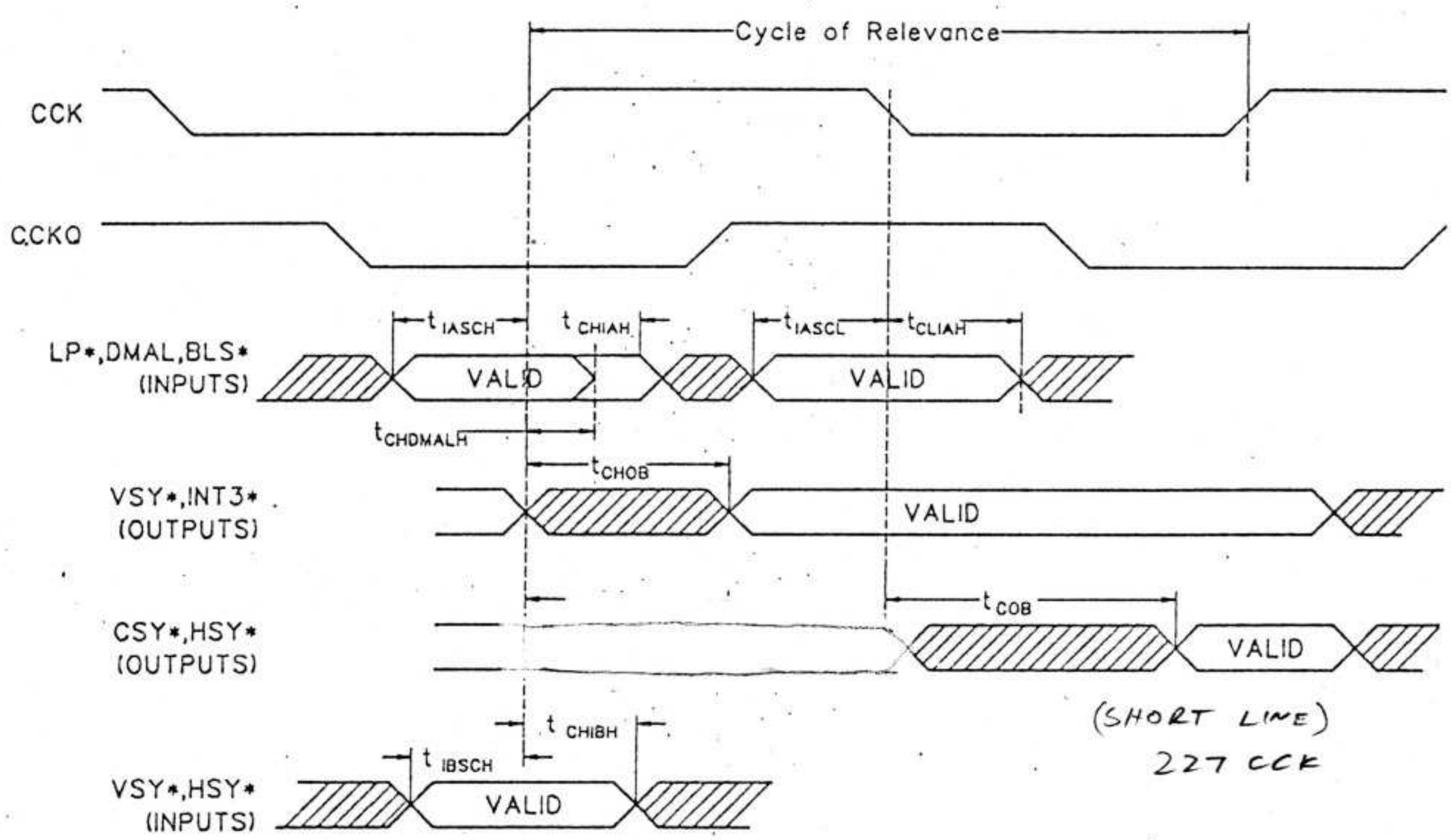
FIGURE 6

MISCELLANEOUS



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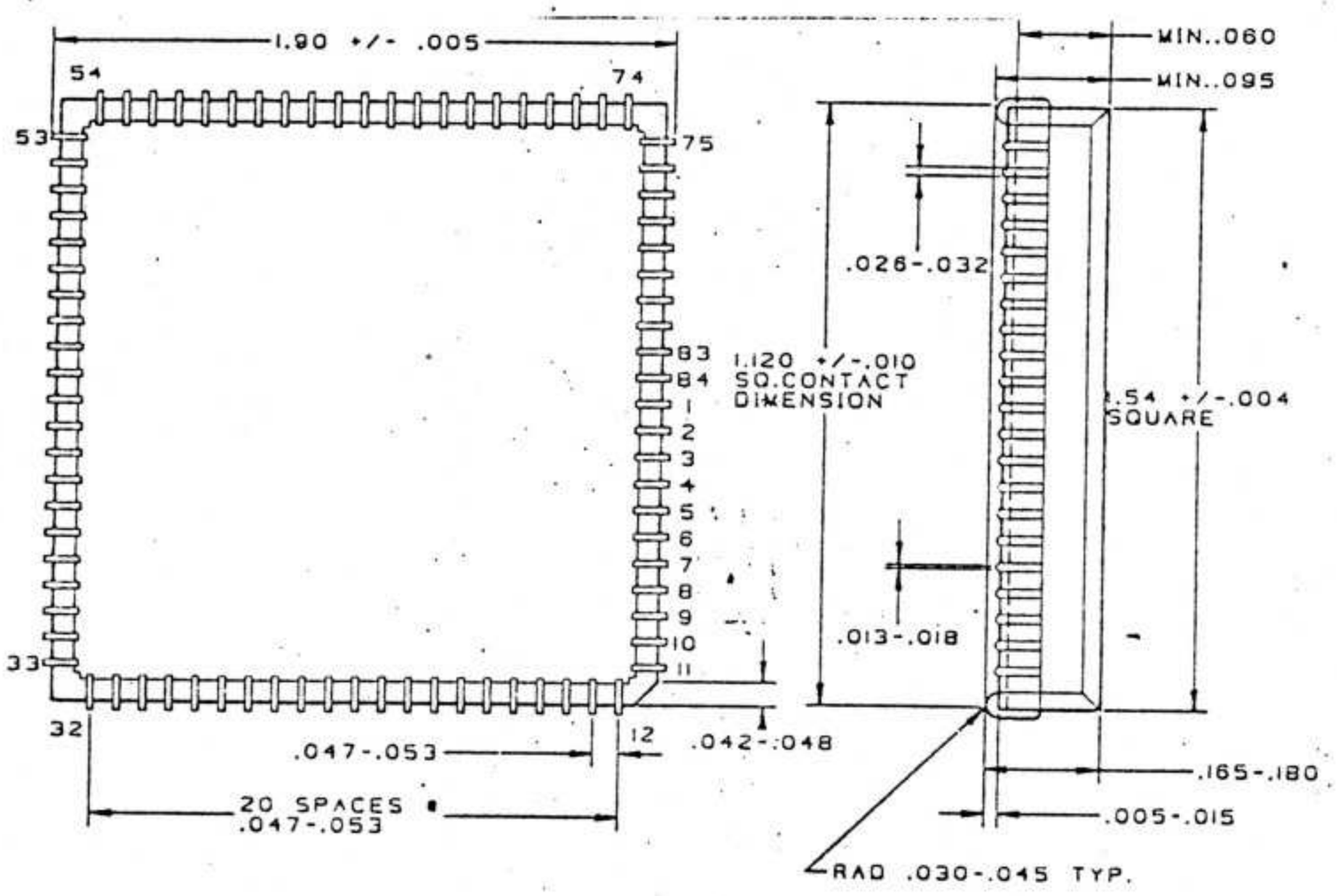
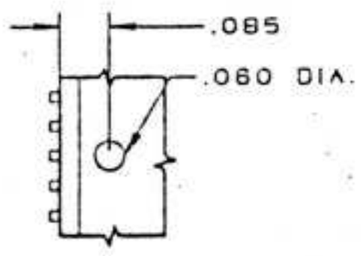
3.0 MECHANICAL REQUIREMENTS

3.1 MARKING

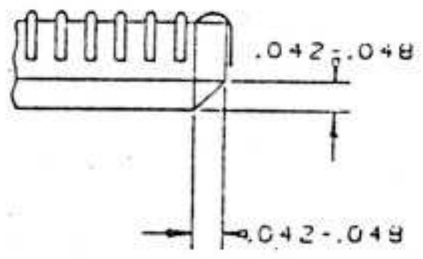
Parts shall be marked with Commodore part number, manufacturer's identification and EIA date code. The device shall be rejected if EIA date code indicates an age of three (3) years or more. Pin No. 1 shall be identified. Refer to Figure 8 for the dimensions of the 84 pin plastic square chip. Dimensions are shown in English units.

FIGURE 8 - CHIP PACKAGE DIMENSIONS





LEAD NO. 1 INDENT



3.2 PROCESS QUALIFICATION TESTS

Integrated Circuits supplied to the requirements of this specification shall also meet the requirements of the latest revision of Commodore Engineering Policy Instruction No. 1.02.008. Support documentation shall be made available by the supplier upon request.

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4.0 MODES OF OPERATION

4.1 GENERAL

This device is an address generator type IC. Its main function is as a RAM address generator and register address encoder that shall produce all DMA addresses from 25 channels.

The block diagram (Figure 2) for this device shows the DMA control and address bus logic. The output of each controller indicates the number of DMA channels driving the Register Address Encoder and RAM Address Generator.

The Register Address Encoder is a simple PLA type of structure that shall produce a predetermined address on the RGA bus whenever one of the DMA channels is active.

The RAM Address Generator contains an 18 bit pointer register for each of the 25 DMA channels and also contains pointer restart (backup) registers and jump registers for six (6) of the channels. A full 18 bit adder carries out the pointer increments and adds for jumps.

The priority control logic looks at the pipelined DMA requests from each controller and stages the DMA cycles based upon their programmed priority and sync counter time slot. Then it signals the processor to get off the bus by asserting the DBR line. The following is a brief description of the device's major operational modes.

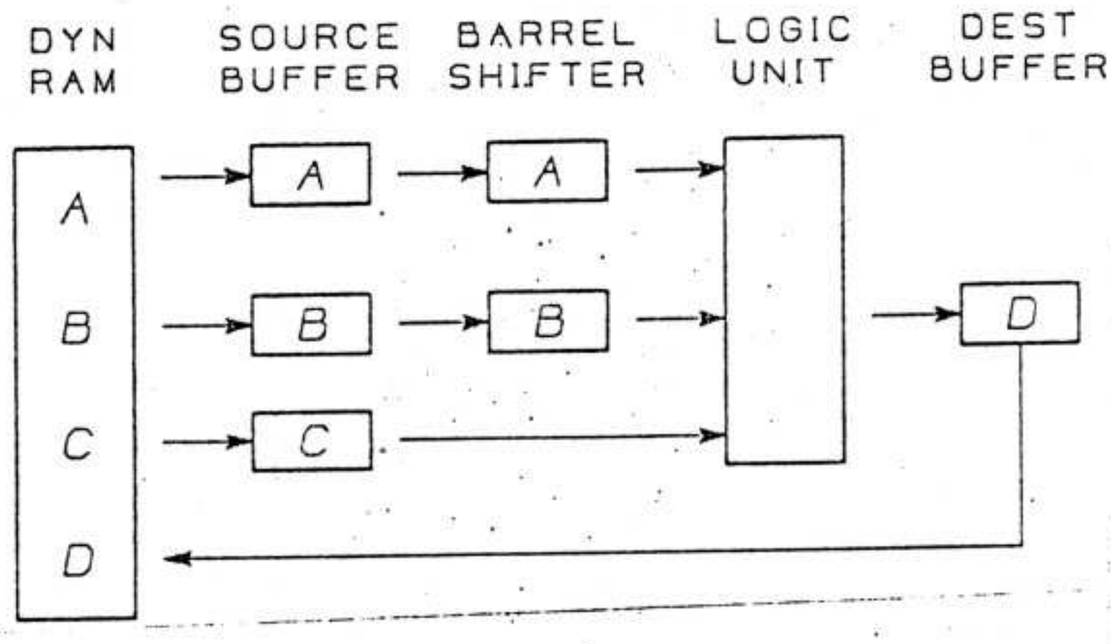
4.2 BLITTER

The procedure for moving and combining bit mapped images in memory received the name Bit Blit from a computer instruction that did block transfers of data on bit boundaries. These routines became known as Bit Blitters or Blitters. The Blitter DMA Controller is preloaded with the address and size of three (3) source images (A, B, and C) and one (1) destination (D) in the dynamic RAM (Refer to Figure 4). These images can be as small as a single character or as large as twice the screen size. They can be full images or smaller windows of a larger image. The actual pixel resolution is controlled by the BLTSIZE register which contains 10 bits for the image height (10 bits = 1024 dots max) and 6 bits for the image width (6 bits = 64 words = 1024 pixels max). After one word of each source image is sequentially loaded into the source buffer (A, B, C) they are shifted and then combined together in the logic unit to perform image movement overlay, masking, and replacements. The result is captured in the destination buffer (D) and sent back to the RAM memory destination address.

This operation is repeated until the complete image has been processed. The unit has extensive pipelining to allow for shifter and logic unit propagation time, while the next set of source words is being fetched.

A control register determines which of 256 possible logic operations is to be performed as the source images are combined and how far they are to be moved (Barrel shifted). In addition to the image combining and movement powers, the Blitter can be programmed to do line drawing or area fill between lines.

FIGURE 9 - BLITTER BLOCK DIAGRAM



4.3 BITPLANE ADDRESSING

Some computer bitmap displays are organized so that the bitplanes for each pixel are all located within the same address. This is called pixel addressing. If the entire data word of one address is used for a single pixel with 8 bit planes, the data word will look like this. (numbers are bitplanes):

12345678---------

The data compression can be improved by packing more than one pixel into a single address like this:

1234567812345678

or like this, if there are only 4 bitplanes:

1234123412341234

The IC device uses a bitmap technique called Bitplane Addressing. This separates the bitplanes in memory. To create a 4 plane (16 color) image, the bitplane display DMA channels fetch from 4 separate areas of memory like this:

1111111111111111
2222222222222222
3333333333333333
4444444444444444

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These are held in buffer registers and are used together as pixels, one bit at a time, by the display (left to right).

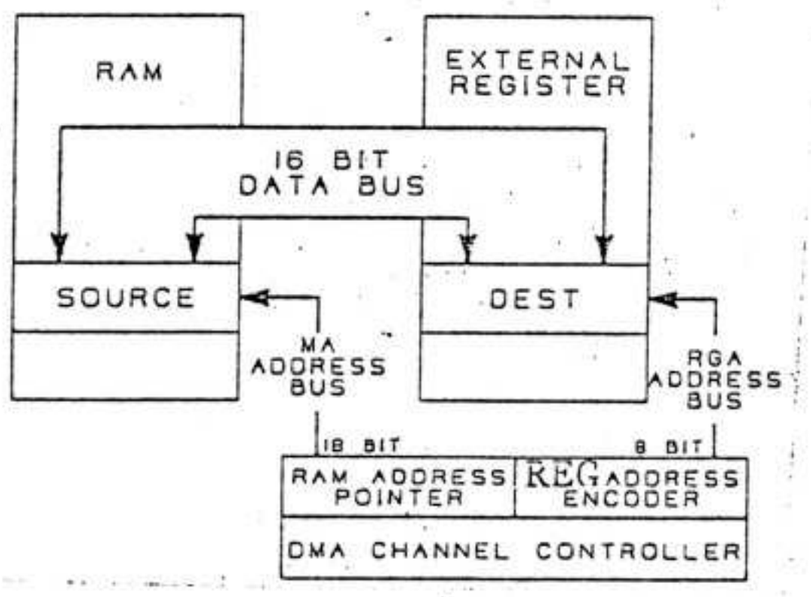
This technique allows reduced odd numbers of bitplanes (such as 3 or 5) while maintaining packing efficiency and speed. It also allows grouping bitplanes into 2 separate images, each with independent hardware high speed image manipulation, line draw, and area fill.

4.4 DMA CHANNEL FUNCTIONS

Each channel has an 18 bit RAM address pointer that is placed on the MA memory address bus and is used to select the location of the DMA data transfer from anywhere in 256K words (512K bytes) of RAM.

An eight (8) bit destination address is simultaneously placed on the register address bus (RGA), sending the data to the corresponding register.
Figure 10 shows a typical DMA channel and almost all channels have RAM as source and chip registers as destination.

FIGURE 10 - DMA CHANNEL (TYPICAL)



The pointer must be preloaded and is automatically incremented each time a data transfer occurs.

Each controller utilizes one or more of these DMA channels for its own purposes. The following is a brief summary of these controllers and the DMA channels they use.

Refer to Appendix A of this specification for raster line time allocation for each of these DMA channels.

A-Blitter (4 Channels)

The Blitter uses four (4) DMA channels, three (3) sources and one (1) destination as previously described.

Once the Blitter has been started, the four (4) DMA channels are synchronized and pipelined to automatically handle the data transfers without further processor intervention. The images are manipulated in memory, independent of the display (bitplane DMA).

B-Bitplane(Six (6) Channels)

The bitplane controller continuously(during display) transfers display data from memory to display buffer registers. There are six (6) DMA channels to handle the data from six (6) independent bit planes. The buffers convert this bitplane data into pixel data for the display.

Each bitplane can be a full image or a window into an image that is up to four (4) times the screen size. They can be grouped into two (2) separate images, each with its own color registers.

C-Copper (One (1) Channel)

The Copper is a co-processor that uses one of the DMA channels to fetch its instructions. The DMA pointer is the instruction counter and must be preloaded with the starting address of Copper's instructions.

The Copper can move (write) data into chip registers. It can skip, jump, and wait (halt). These simple instructions give great power and flexibility because of the following features.

When the Copper is halted, it is off the data bus, using no bus cycles until the wait is over. The programmed wait value is compared to a counter that keeps track of the TV beam position (Beam Counter) and when they are equal, the Copper will resume fetching instructions.

It can cause interrupts, reload the color registers, start the Blitter or service the audio. It can modify almost any register inside or outside the IC device, based on the TV screen coordinates given by the Beam Counter and the actual address encoded on the RGA bus.

D-Audio (Four (4) Channels)

There are four (4) audio channels, all of which are located outside of the DMA Controller IC. Each controller is independent and uses one DMA channel from the DMA Controller IC and fetches

its data during a dedicated timing slot within horizontal blanking. This is accomplished by a controller asserting the DMAL input on the DMA Controller.

E-Sprites (Eight (8) Channels)

There are eight (8) independent Sprite controllers, each with its own DMA channel and its own dedicated time slot for DMA data transfer. Sprites are line buffered objects that can move very fast because their position is controlled by hardware registers and comparators.

Each Sprite has two (2) 16 bit data registers, located outside the device, that define a 16 pixel wide Sprite with four (4) colors. Each has a horizontal position register (also located outside the device), a vertical start position register, aqnd a vertical stop position register. This allows variable vertical size sprites.

The Sprite DMA controller fetches image and position data automatically from anywhere in 512K of memory.

Sprites can be run automatically in DMA mode or they can be loaded and controlled by the microprocessor.

Each Sprite can be reused vertically as often as desired. Horizontal reusing is also possible with microprocessor control.

F-Disk (One (1) Channel)

The disk controller, which is located outside of the DMA controller, uses a single DMA channel from the device. The controller uses this DMA time slot for data transfer and can read or write a block of data up to 128K anywhere in 512K of memory.

G-Memory Refresh (One (1) Channel)

The refresh controller uses a single DMA channel with its own time slots. It places RAS addresses on the memory address bus (MAs) during these slots, in order to refresh the dynamic RAM. Memory is refresh on every raster line.

During the DMA no data transfer actually takes place. The register address bus (RGA) is used to supply video synchronizing codes. At this time RASO* and RASI* are low and CASU* and CASL* are inactive.

4.5 RAM AND REGISTER ADDRESSING

The device generates RAM addresses from two sources, the processor

or from the device performing DMA cycles, selected by a multiplexer. This multiplexer allows the processor to access RAM when AS* and RAMEN* are both low. At this time, the device also multiplexes the processor address (A1-A18) onto the MA bus. The device places A1 to A8 & A17 on the MA0 to MA9 outputs, respectively, during the row address time and places A9 to A16 & A18 on the MA0 to MA9, respectively, during the column address time. The A19 line is used by the IC to determine which RAS line is to be asserted. If A19 is low, RAS0* is enabled, and if high, RAS1* is enabled. The device also senses the LDS* and UDS* inputs to determine which CAS to drop. If LDS* is low, the IC will drop CASL* and if UDS* is low, CASU* is dropped.

When the device needs to do a DMA cycle, the multiplexer disables the processor from accessing RAM by asserting the Data Bus Request Line (DBR*). At this time, the device multiplexes its generated RAM address onto the MA lines and will only make RAS0* go low, unless it is a refresh cycle where RAS1* will also go low. During a DMA cycle, the IC device will also assert both CASU* and CASL*, unless it is a refresh cycle where they both remain inactive.

The device also generates RGA addresses from either the processor or device DMAs, each of which is selected by another internal multiplexer. This multiplexer allows the processor to perform a register read/write access when AS* and RGEN* are both low. The device then takes the low order byte of the processor address A1 to A8 and reflects its value on the RGA output bus RGA1 to RGA8. The device will reflect the status of PRW input on the RRW output line, to indicate a memory read or write operation.

During a device DMA cycle, the multiplexer prevents the processor from doing a register access by asserting the DBR* line. The device will then place the contents of its register address encoder onto the RGA bus.

5.0 REGISTER DESCRIPTION

This DMA controller device contains 97 registers that can be accessed after the following conditions have been met. The state of AS* and RGEN* must be an active low level and the least 8 significant address bits (A1 thru A8) must contain the valid address of the register to be accessed. Refer to Table 2 for complete list of register addresses and type.

The following is a detailed description of the register set.

REGISTER	FUNCTION
AUD x LCH	Audio channel x location (high 3 bits)
AUD x LCL	Audio channel x location (low 15 bits)

This pair of registers contains the 18 bit starting address (location) of Audio channel x (x=0,1,2,3) DMA data. This is not a pointer register and therefore only needs to be reloaded if a diferent memory location is to be outputted.

BLT x PTH	Blitter pointer to x (high 3 bits)
BLT x PTL	Blitter pointer to x (low 15 bits)

This pair of registers contains the 18 bit address of Blitter source (x=A,B,C) or dest. (x=D) DMA data. This pointer must be preloaded with the starting address of the data to be processed by the blitter. After the Blitter is finished it will contain the last data address (plus increment and modulo).

LINE DRAW: BLTAPTL is used as an accumulator register and must be preloaded with the starting value of (2Y-X) where Y/X is the line slope. BLTCPT and BLTDPT (both H and L) must be preloaded with the starting address of the line.

BLT x MOD — Blitter Modulox

This register contains the Modulo for Blitter source (x=A,B,C) or Dest (x=D). A Modulo is a number that is automatically added to the address then points to the start of the next line. Each source or destination has its own Modulo, allowing each to be a different size, while an identical area of each is used in the Blitter operation.

LINE DRAW: BLTAMOD and BLTBMOD are used as slope storage registers and must be preloaded with the values (4Y-4X) and (4Y) respectively. Y/X=line slope BLTCMOD and BLTDMOD must both be preloaded with the width (in bytes) of the image into which the line is being drawn. (normally 2 times the screen width in words)

BLTAFWM	Blitter firstword mask for Source A
BLTALWM	Blitter last word mask for Source A

The patterns in these two registers are "anded" with the first and last words of each line of data from Source A into the Blitter. A zero in any bit overrides data from Source A. These registers should be set to all "ones" for fill mode or for line drawing mode.

BLTxDAT — Blitter source x data register

This register holds Source x (x=A,B,C) data for use by the Blitter. It is normally loaded by the Blitter DMA channel, however, it may also be preloaded by the microprocessor.
LINE DRAW: BLTADAT is used as an index register and must be preloaded with 8000.
BLTBDAT is used for texture. It must be preloaded with FF if no texture (solid line) is desired.

BLTDDAT — Blitter destination data register

This register holds the data resulting from each word of Blitter operation until it is sent to a RAM destination. This is a dummy address and cannot be read by the micro. The transfer is automatic during Blitter operation.

BLTCON0 — Blitter control register 0
BLTCON1 — Blitter control register 1

These two control registers are used together to control Blitter operations. There are 2 basic modes, area and line, which are selected by bit 0 of BLTCON1, as shown below.

AREA MODE ("normal")

BIT#	BLTCON0	BLTCON1
15	ASH3	BSH3
14	ASH2	BSH2
13	ASH1	BSH1
12	ASA0	BSH0
11	USEA	X
10	USEB	X
09	USEC	X
08	USED	X
07	LF7	X
06	LF6	X
05	LF5	X
04	LF4	EFE
03	LF3	IFE
02	LF2	FCI
01	LF1	DESC
00	LF0	LINE(=0)

ASH3-0 Shift value of A source
BSH3-0 Shift value of B source
USEA Mode control bit to use Source A
USEB Mode control bit to use Source B
USEC Mode control bit to use Source C

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USED Mode control bit to use Destination D
LF7-0 Logic function minterm select lines
EFE Exclusive fillenable
IFE Inclusive fill enable
FCI Fill carry input
DESC Descending (decreasing address) control bit
LINE Line mode control bit (set to 0)

LINE DRAW: LINE MODE (line draw)

BIT#	BLTCONO	BLTCONI
15	START3	0
14	START2	0
13	START1	0
12	START0	0
11	1	0
10	0	0
09	1	0
08	1	0
07	LF7	0
06	LF6	SIGN
05	LF5	OVF
04	LF4	SUD
03	LF3	SUL
02	LF2	AUL
01	LF1	SING
00	LF0	LINE(=1)

START3-0 Starting point of line (0 thru 15 hex)
LF7-0 Logic function minterm select lines
should be preloaded with 4A in order

to select the equation $D=(\bar{A}C+AB\bar{C})$. Since A contains a single bit truee (8000), most bits will pass the C field unchanged (not A and C), but one bit will invert the C Field and combine it with texture (A and B and not C). The A bit is automatically moved across the word by the hardware.

LINE Line mode control bit (set to 1)
SIGN Sign flag
OVF Word overflow flag
SING Single bit per horiz. line
for use with subsequent Area Fill
SUD Sometimes Up or Down (=AUD*)
SUL Sometimes Up or Left
AUL Always Up or Left
The 3 bits above select the Octant for

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line draw:

OCT	SUD	SUL	AUL
0	1	1	0
1	0	0	1
2	0	1	1
3	1	1	1
4	1	0	1
5	0	1	0
6	0	0	0
7	1	0	0

BLTSIZE — Blitter start and size (Window, width height)

This register contains the width and height of the blitter operation (in line mode width must=2, height = line length) Writing to this register will start the Blitter, and should be done last, after all pointers and control registers have been initialized.

BIT# 15, 14, 13, 12, 11, 10, 09, 08, 07, 06, 05, 04, 03, 02, 01, 00
h9 h8 h7 h6 h5 h4 h3 h2 h1 h0, w5 w4 w3 w2 w1 w0

h=Height=Vertical lines (10 bits=1024 lines max)
w=Width =Horiz pixels (6 bits=64 words=1024 pixels max)

LINE DRAW: BLTSIZE controls the line length and starts the line draw when written to. The h field controls the line length (10 bits gives lines up to 1024 dots long). The w field must be set to 02 for all line drawing.

BPLxPTH — Bit plane x pointer (high 3 bits)
BPLxPTL — Bit plane x pointer (low 15 bits)

This pair of registers contains the 18 bit pointer to the address of Bit plane x (x=1,2,3,4,5,6) DMA data. This pointer must be reinitialized by the processor or Copper to point to the beginning of Bit Plane data every vertical blank time.

BPL1MOD — Bit plane modulo (odd planes)
BPL2MOD — Bit plane modulo (even planes)

These registers contain the Modulos for the odd and even bit planes. A Modulo is a number that is automatically added to the address at the end of each line, in order that the address then points to the start of the next line. Since they have separate modulos, the odd and even bit planes may have sizes that are different from each other, as well as different from the Display Window size.

BPLCONO — Bit plan control register (miscellaneous control bits)

This register controls the operation of the Bit Planes and various

aspects of the display.

BIT#	BPLCONO
15	HIRES
14	BPU2
13	BPU1
12	BPU0
11	HOMOD
10	DBLPF
09	COLOR
08	GAUD
07	X
06	X
05	X
04	X
03	LPEN
02	LACE
01	ERSY
00	X

HIRES=High resolution (640) mode
BPU =Bit-plane use code 000-110 (NONE through 6 inclusive)
HOMOD=Hold and Modify mode
DBLPF=Double playfield (PF1=odd PF2=even bit planes)
COLOR=Composite video COLOR enable
GAUD=Genlock audio enable (mixed on BKGND pin during vertical blanking
LPEN=Light pen enable (reset on power up)
LACE=Interlace enable (reset on power up)
ERSY=External Resync (HSYNC, VSYNC pads become inputs) (reset on power up)

COPCON Copper control register

This is a 1 bit register that when set true, allows the Copper to access the Blitter hardware. This bit is cleared by power on reset, so that the Copper cannot access the Blitter hardware.

BIT#	NAME	FUNCTION
01	CDANG	Copper danger mode. Allows Copper access to Blitter if true.

COPJMP1 Copper restart at first location
COPJMP2 Copper restart at second location

These addresses are strobe addresses, that when written to cause the Copper to jump indirect using the address contained in the First or Second Location registers described below. The Copper itself can write to these addresses, causing its own jump indirect.

COP1LCH	Copper first location register (high 3 bits)
COP1LCL	Copper first location register (low 15 bits)
COP2LCH	Copper second location register (high 3 bits)
COP2LCL	Copper second location register (low 15 bits)
COPINS	Copper instruction fetch identify

This is a dummy address that is generated by the Copper whenever it is loading instructions into its own instruction register. This actually occurs every Copper cycle except for the second (IR2) cycle of the MOVE instruction. The Three types of instructions are shown below.

MOVE	Move immediate to dest
WAIT	Wait until beam counter is equal to, or greater than. (keeps Copper off of bus until beam position has been reached)
SKIP	Skip if beam counter is equal to, or greater than. (skips following MOVE inst. unless beam position has been reached)

	MOVE		WAIT UNTIL			SKIP IF		
BIT#	IR1	IR2	IR1	IR2		IR1	IR2	
15	X	RD15	VP7	BFD	*	VP7	BFD	*
14	X	RD14	VP6	VE6		VP6	VE6	
13	X	RD13	VP5	VE5		VP5	VE5	
12	X	RD12	VP4	VE4		VP4	VE4	
11	X	RD11	VP3	VE3		VP3	VE3	
10	X	RD10	VP2	VE2		VP2	VE2	
09	X	RD09	VP1	VE1		VP1	VE1	
08	DA8	RD08	VP0	VE0		VP0	VE0	
07	DA7	RD07	HP8	HE8		HP8	HE8	
06	DA6	RD06	HP7	HE7		HP7	HE7	
05	DA5	RD05	HP6	HE6		HP6	HE6	
04	DA4	RD04	HP5	HE5		HP5	HE5	
03	DA3	RD03	HP4	HE4		HP4	HE4	
02	DA2	RD02	HP3	HE3		HP3	HE3	
01	DA1	RD01	HP2	HE2		HP2	HE2	
00	0	RD00	1	1		1	1	

IR1=First instruction register
IR2=Second instruction register
DA =Destination Address for MOVE instruction. Fetched during IR1 time, used during IR2 time on RGA bus.
RD =RAM data moved by MOVE instruction at IR2 time directly from RAM to the address given by the DA field.
VP =Vertical Beam Position comparison bit
HP =Horizontal Beam Position comparison bit
VE =Enable comparison (mask bit)
HE =Enable comparison (mask bit)

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*NOTE BFD=Blitter finished disable. When this bit is true, the Blitter Finished flag will have no effect on the Copper. When this bit is zero the Blitter Finished flag must be true (in addition to the rest of the bit comparisons) before the Copper can exit from its wait state, or skip over an instruction. Note that the V7 comparison cannot be masked.

The Copper is basically a 2 cycle machine that requests the bus only during odd memory cycles. (4 memory cycles per in) This prevents collisions with Display, Audio, Disk, Refresh, and Sprites, all of which use only even cycles. It therefore needs (and has) priority over only the Blitter and Micro.

There are only three types of instructions: MOVE immediate, WAIT until, and SKIP if. All instructions (except for WAIT) require 2 bus cycles (and two instruction words). Since only the odd bus cycles are requested, 4 memory cycle times are required per instruction. (memory cycles are 280 ns)

There are two indirect jump registers COP1LC and COP2LC. These are 18 bit pointer registers whose contents are used to modify the program counter for initialization or jumps. They are transferred to the program counter whenever strobe addresses COPJMP1 or COPJMP2 are written. In addition COP1LC is automatically used at the beginning of each vertical blank time.

It is important that one of the jump registers be initialized and its jump strobe address hit, after power up but before Copper DMA is initialized. This insures a determined startup address and state.

DIWSTRT	Display window start (upper left vertical-horizontal positon)
DIWSTOP	Display window stop (lower right vertical-horizontal position)

These registers control the Display window size and position, by locating the upper left and lower right corners.
BIT# 15,14,13,12,11,10,09,08,07,06,05,04,03,02,01,00
USE V7 V6 V5 V4 V3 V2 V1 V0 H7 H6 H5 H4 H3 H2 H1 H0
DIWSTRT is vertically restricted to the upper 2/3 of the display (V8=0), and horizontally restricted to the left 3/4 of the display (H8=0).
DIWSTOP is vertically restricted to the lower 1/2 of the display (V8=/=V7), and horizontally restricted to the right 1/4 of the display (H8=1).

DDFSTRT	Display data fetch start (horiz.position)
DDFSTOP	Display data fetch stop (horiz.position)

These registers control the horizontal timing of the beginning and

end of the Bit Plane DMA display data fetch. The vertical Bit Plan DMA timing is identical to the Display windows described above. The Bit Plan Modulos are dependent on the Bit Plane horizontal size, and on this data fetch window size.

Register bit assignment

BIT#	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
USE	X	X	X	X	X	X	X	X	HB	H7	H6	H5	H4	H3	X	X

(X bits should always be driven with 0 to maintain upward compatibility)

The tables below show the start and stop timing for different register contents.

DDFSTRT(Left edge of display data fetch)

PURPOSE	H8,H7,H6,H5,H4
Extra wide (max) *	0 0 1 0 1
wide	0 0 1 1 0
normal	0 0 1 1 1
narrow	0 1 0 0 0

DDFSTOP (Right edge of display data fetch)

PURPOSE	H8,H7,H6,H5,H4
narrow	1 1 0 0 1
normal	1 1 0 1 0
wide (max)	1 1 0 1 1

DMACON	DMA control write (clear or set)
DMACONR	DMA control (and Blitter status) read

This register controls all of the DMA channels, and contains Blitter DMA status bits.

BIT#	FUNCTION	DESCRIPTION
15	SET/CLR	Set/Clear control bit. Determines if bits written with a 1 get set or cleared.
14	BBUSY	Blitter busy status bit (read only)
13	BZERO	Blitter logic zero status bit. (read only)
12	X	
11	X	
10	BLTPRI	Blitter DMA priority (over CPU micro) (also called "Blitter Nasty") (disables /BLS pin, preventing micro from stealing any bus cycles while blitter DMA is running)
09	DMAEN	Enable all DMA below
08	DPLEN	Bit Plane DMA enable
07	COPEN	Copper DMA enable

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06	BLTEN	Blitter DMA enable
05	SPREN	Sprite DMA enable
04	DSKEN	Disk DMA enable
03	AUD3EN	Audio channel 3 DMA enable
02	AUD2EN	Audio channel 2 DMA enable
01	AUD1EN	Audio channel 1 DMA enable
00	AUD0EN	Audio channel 0 DMA enable

DSKPTH — Disk pointer (high 3 bits)
DSKPTL — Disk pointer (low 15 bits)

This pair of registers contains the 18 bit address of Disk DMA data. These address registers must be initialized by the processor or Copper before disk DMA is enabled.

REFPTR — Refresh pointer

This register is used as a Dynamic RAM refresh address generator. It is writeable for test purposes only, and should never be written by the microprocessor.

SPRxPTH — Sprite x pointer (high 3 bits)
SPRxPTL — Sprite x pointer (low 15 bits)

This pair of registers contains the 18 bit address of Sprite x (x=0,1,2,3,4,5,6,7) DMA data. These address registers must be initialized by the processor or Copper every vertical blank time.

SPRxPOS — Sprite x vertical-horizontal position data
SPRxCTL — Sprite x vertical-horizontal

These 2 registers work together as position, size and feature Sprite control registers. They are usually loaded by the Sprite DMA channel, during horizontal blank, however they may be loaded by either processor any time.

SPRxPOS register:

BIT#	SYM	FUNCTION
15-08	SV7-SV0	Start vertical value. High bit (SV8) is in SPRxCTL reg below.
07-00	SH8-SH1	Start horizontal value. Low bit (SH0) is in SPRxCTL reg. below.

SPRxCTL register (writing this address dissables sprite horizontal comparator circuit):

BIT#	SYM	FUNCTION
15-08	EV7-EV0	End (stop) vert.value.low 8 bits
07	ATT	Sprite attach control bit (odd sprites)

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06-04	X	Not used
02	SV8	Start vert.. value high bit
01	EV8	End (stop) vert. value high bit
00	SH0	Start horiz. value Low bit

VPOSR	Read vertical most significant bit (and frame flop)
VPOSW	Write vertical most significant bit (and frame flop)

```
BIT#  15,14,13,12,11,10,09,08,07,06,05,04,03,02,01,00
USE   LOF---------------------------------------- V8
```

LOF=Long frame (auto toggle control bit in BPLCONO)

VHPOSR	Read vertical and horizontal position of beam or lightpen
VHPOSW	Write vertical and horizontal position of beam or lightpen

```
BIT#  15,14,13,12,11,10,09,08,07,06,05,04,03,02,01,00
USE   V7 V6 V5 V4 V3 V2 V1 V0,H8 H7 H6 H5 H4 H3 H2 H1
```

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TABLE 2 - REGISTER ADDRESSES

NAME*	ADDRESS** A8 thru A0	TYPE***	DESCRIPTION
BLTDDAT	&*000	ER	Blitter destination (dummy address)
DMACONR	*002	R	DMA control (and Blitter status)
VPOSR	*004	R	Read Vertical - MSB
VHPOSR	*006	R	Read Vertical and horizontal Position of beam.
DSKPTH	+*020	W	Disk pointer (High (3) bits)
DSKPTL	+*022	W	Disk pointer (Low 15 bits)
REFPTR	&*028	W	Refresh pointer.
VPOSW	*02A	W	Write Vertical MSB
VHPOSW	*02C	W	Write Vertical and horizontal Position of beam
COPCON	*02E	W	Co-processor control register
STREOU	&*038	S	Strobe for horizontal sync. with VB and EQU
STRVBL	&*03A	S	Strobe for horizontal sync. with VB
STRHOR	&*03C	S	Strobe for horizontal sync.
STRLONG	&*03E	S	Strobe for identification of long horizontal line
BLTCONO	-040	W	Blitter control register 0
BLTCON1	-042	W	Blitter
BLTAFWM	-044	W	Blitter first word mask for source A
BLTALWM	-046		Blitter last word mask for source A
BLTCPTH	+-048	W	Blitter pointer to source C (High 3 bits)
BLTCPTL	+-04A	W	Blitter pointer to source C (Low 15 bits)
BLTBPTH	+-04C	W	Blitter pointer to source B (High 3 bits)
BLTBPTL	+-04E	W	Blitter pointer to source B (Low 15 bits)
BLTAPTH	+-050	W	Blitter pointer to source A (High 3 bits)
BLTAPTL	+-052	W	Blitter pointer to source A (low 15 bits)
BLTDPTH	+-054	W	Blitter pointer to destination D (High 3 bits)
BLTDPTL	+-056	W	Blitter pointer to destination D (Low 15 bits)
BLTSIZE	-058	W	Blitter start and size (window, width and height)
BLTCMOD	-060	W	Blitter modulo for source C

TABLE 2 -REGISTER ADDRESSES (cont"d) (2)

BLTBMOD	-062	W	Blitter modulo for source B
BLTAMOD	-064	W	Blitter modulo for source A
BLTDMOD	-066	W	Blitter modulo for destination D
BLTCDAT	&-070	W	Blitter source C data register
BLTBDAT	&-072	W	Blitter source B data register
BLTADAT	&-074	W	Blitter source A data register
COP1LCH	+080	W	Co-processor first location register (High 3 bits)
COP1LCL	+082	W	Co-processor first location register (Low 15 bits)
COP2LCH	+084	W	Co-processor second location register (High 3 bits)
COP2LCL	+086	W	Co-processor second location register (Low 15 bits)
COPJMP1	088	S	Co-processor restart at first location
COPJMP2	08A	S	Co-processor restart at second location
COPINS	08C	W	Co-processor instruction fetch identify
DIWSTRT	08E	W	Display window start (upper vertical -horizontal position)
DIWSTOP	090	W	Display window stop (lower right vertical-horizontal position)
DDFSTRT	092	W	Display bit plane data fetch start (horizontal position)
DDFSTOP	094	W	Display bit plane data fetch stop (horizontal position)
DMACON	096	W	DMA control write (clear or set)
INTENA	09A	W	Interrupt Enable bits (clear or set bits)
INTREQ	096	W	Interrupt Request bits (clear or set bits)
AUDOLCH	+0A0	W	Audio channel 0 location (High 3 bits)
AUDOLCL	+0A2	W	Audio channel 0 location (Low 15 bits)
AUD1LCH	+0B0	W	Audio channel 1 location (High 3 bits)
AUD1LCL	+0B2	W	Audio channel 1 location (Low 15 bits)
AUD2LCH	+0C0	W	Audio channel 2 location (High 3 bits)
AUD2LCL	+0C2	W	Audio channel 2 location (Low 15 bits)
AUD3LCH	+0D0	W	Audio channel 3 location (High 3 bits)
AUD3LCL	+0D2	W	Audio channel 3 location (Low 15 bits)
BL1PTH	+0E0	W	Bit plane 1 pointer (High 3 bits)
BL1PTL	+0E2	W	Bit plane 1 pointer (Low 15 bits)
BPL2PTH	+0E4	W	bit plane 2 pointer (High 3 bits)
BPL2PTL	+0E6	W	Bit plane 2 pointer (Low 15 bits)
BPL3PTH	+0E8	W	Bit plane 3 pointer (High 3 bits)
BPL3PTL	+0EA	W	Bit plane 3 pointer (Low 15 bits)

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TABLE 2 - REGISTER ADDRESSES (cont'd) (3)

BPL4PTH	+0EC	W	Bit plane 4 pointer (High 3 bits)
BPL4PTL	+0EE	W	Bit plane 4 pointer (Low 15 bits)
BPL5PTH	+0F0	W	Bit plane 5 pointer (High 3 bits)
BPL5PTL	+0F2	W	Bit plane 5 pointer (Low 15 bits)
BPL6PTH	+0F4	W	Bit plane 6 pointer (High 3 bits)
BPL6PTL	+0F6	W	Bit plane 6 pointer (Low 15 bits)
BPLCONO	100	W	Bit plane control register (miscellaneous control bits)
BPL1MOD	108	W	Bit plane modulo (Odd planes)
BPL2MOD	10A	W	Bit plane modulo (Even planes)
SPR0PTH	+120	W	Sprite 0 pointer (High 3 bits)
SPR0PTL	+122	W	Sprite 0 pointer (Low 15 bits)
SPR1PTH	+124	W	Sprite 1 pointer (High 3 bits)
SPR1PTL	+126	W	Sprite 1 pointer (Low 15 bits)
SPR2PTH	+128	W	Sprite 2 pointer (High 3 bits)
SPR2PTH	+12A	W	Sprite 2 pointer (Low 15 bits)
SPR3PTH	+12C	W	Sprite 3 pointer (High 3 bits)
SPR3PTL	+12E	W	Sprite 3 pointer (Low 15 bits)
SPR4PTH	+130	W	Sprite 4 pointer (High 3 bits)
SPR4PTL	+132	W	Sprite 4 pointer (Low 15 bits)
SPR5PTH	+134	W	Sprite 5 pointer (High 3 bits)
SPR5PTL	+136	W	Sprite 5 pointer (Low 15 bits)
SPR6PTH	+138	W	Sprite 6 pointer (High 3 bits)
SPR6PTL	+13A	W	Spirte 6 pointer (Low 15 bits)
SPR7PTH	+13C	W	Sprite 7 pointer (High 3 bits)
SPR7PTL	+13E	W	Sprite 7 pointer (Low 15 bits)
SPR0POS	%140	W	Sprite 0 vertical-horizontal start position data
SPR0CTL	%142	W	Sprite 0 vertical stop position and control data.
SPR1POS	%148	W	Sprite 1 vertical-horizontal start position data
SPR1CTL	%14A	W	Sprite 1 vertical stop position and control data.
SPR2POS	%150	W	Sprite 2 vertical-horizontal start position data
SPR2CTL	%152	W	Sprite 2 vertical stop position and control data.
SPR3POS	%158	W	Sprite 3 vertical-horizontal start position data.
SPR3CTL	%15A	W	Sprite 3 vertical stop position and control data.
SPR4POS	%160	W	Sprite 4 vertical-horizontal start position data.
SPR4CTL	%160	W	Sprite 4 vertical stop position and control data.
SPR5POS	%168	W	Sprite 5 vertical-horizontal start position data.

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TABLE 2 - REGISTER ADDRESSES (CONT'D) (4)

SPR5CTL	%16A	W	Sprite 5 vertical stop position and control data.
SPR6POS	%170	W	Sprite 6 vertical-horizontal start position data.
SPR6CTL	%172	W	Sprite 6 vertical stop position and control data.
SPR7POS	%178	W	Sprite 7 vertical-horizontal start position data.
SPR7CTL	%17A	W	Sprite 7 vertical stop position and control data.

* PTL and PTH - 18 bit pointer that addresses DMA data must be reloaded by a processor before use. (Vertical blank for Bit Plane and Sprite pointers and prior to starting the Blitter for Blitter pointers.)

LCL and LCH - 18 bit location (starting address) of DMA data. Used to automatically restart pointers, such as the co-processor program counter (during vertical blank) and the Audio sampler counter (whenever the audio length count is finished.

MOD - 15 bit modulo. A number that is automatically added to the memory address at the end of each line to generate the address for for the beginning of the next line. This allows the Blitter (or the Display Window) to operate on (or display) a window of data that is smaller than the actual picture in memory (memory map). Uses 15 bits plus sign extended.

** & Register used by DMA channel only

% Register used mostly by DMA channel and processor sometimes.

+ Address register pair. Low word uses DB1-DB15. High word uses DB0-DB2.

* Address not writeable by co-processor.

- Address not writeable by co-processor, unless COPON is set true.

*** W = Write
R = Read
S = Strobe
ER = Early Read

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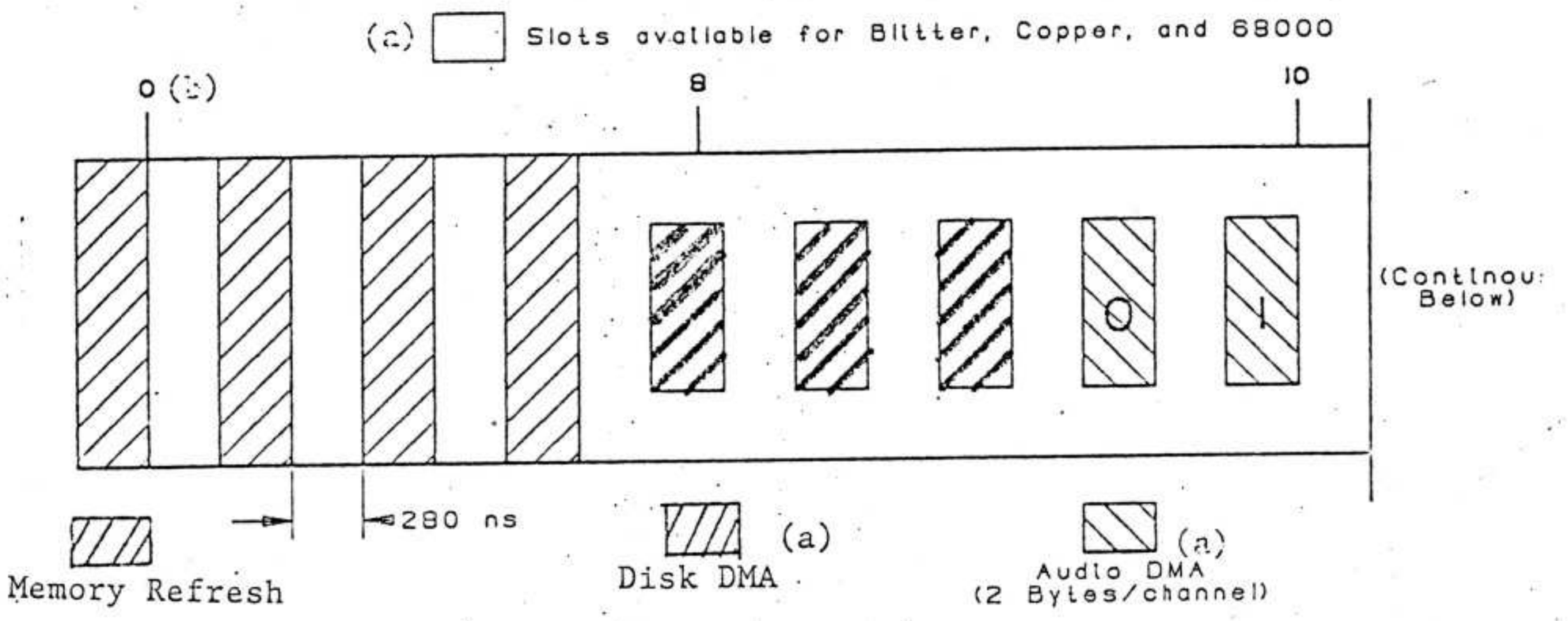
APPENDIX A

DMA TIME SLOT ALLOCATION / HORIZONTAL LINE



a. These operations only take slots if the associated operation is being performed.
   NOTE: Copper Data Move instructions require four (4) slots.
   Copper Wait instructions require six (6) slots.

b. This cycle 0 appears to exclude one of the memory refresh cycles. This is not the case.

   Actual system hardware demands certain specific values for data fetch start and display start. Therefore this timing chart has been adjusted to match those requirements.

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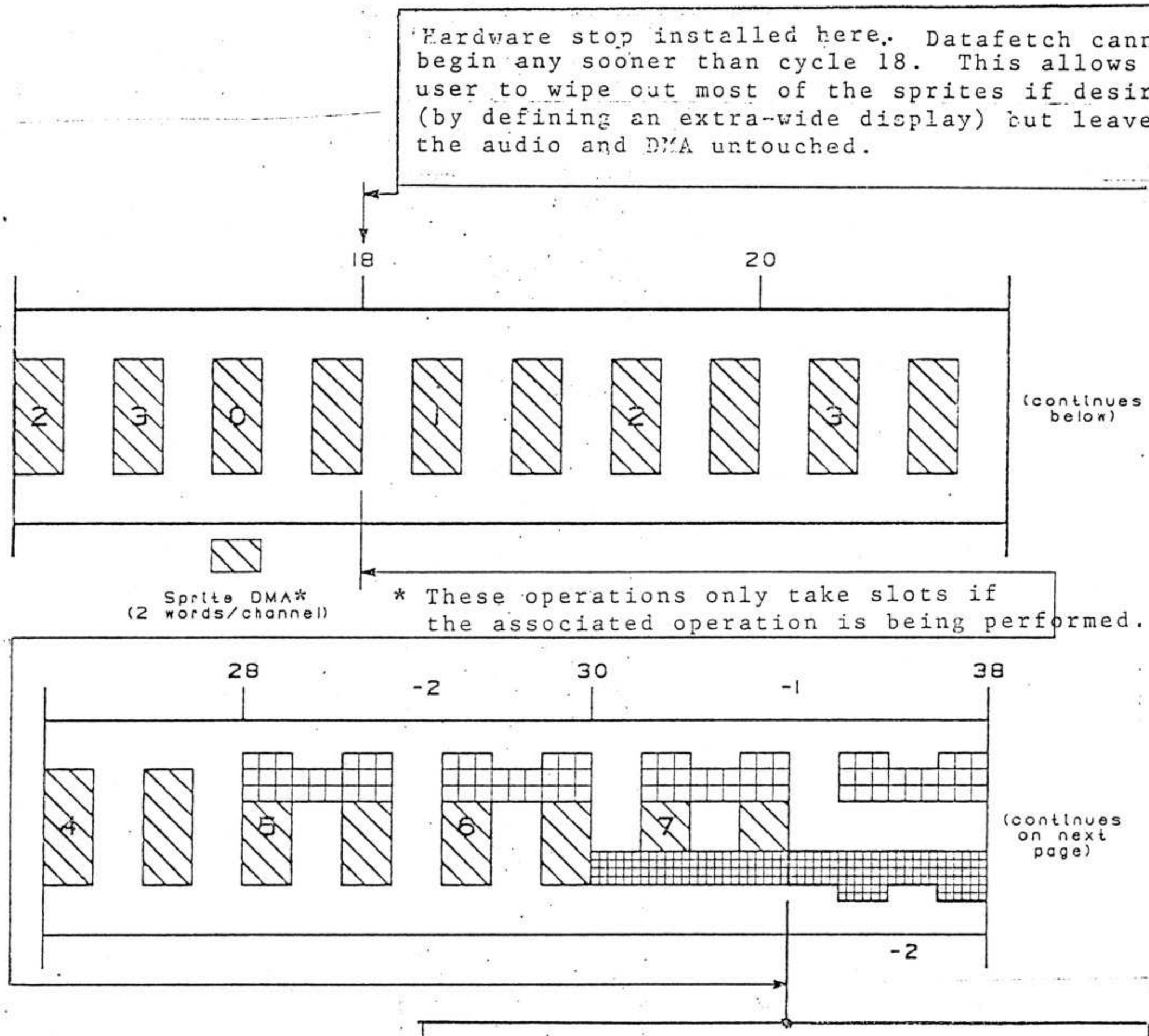
DMA Time Slot Allocation / Horizontal line (cont.)



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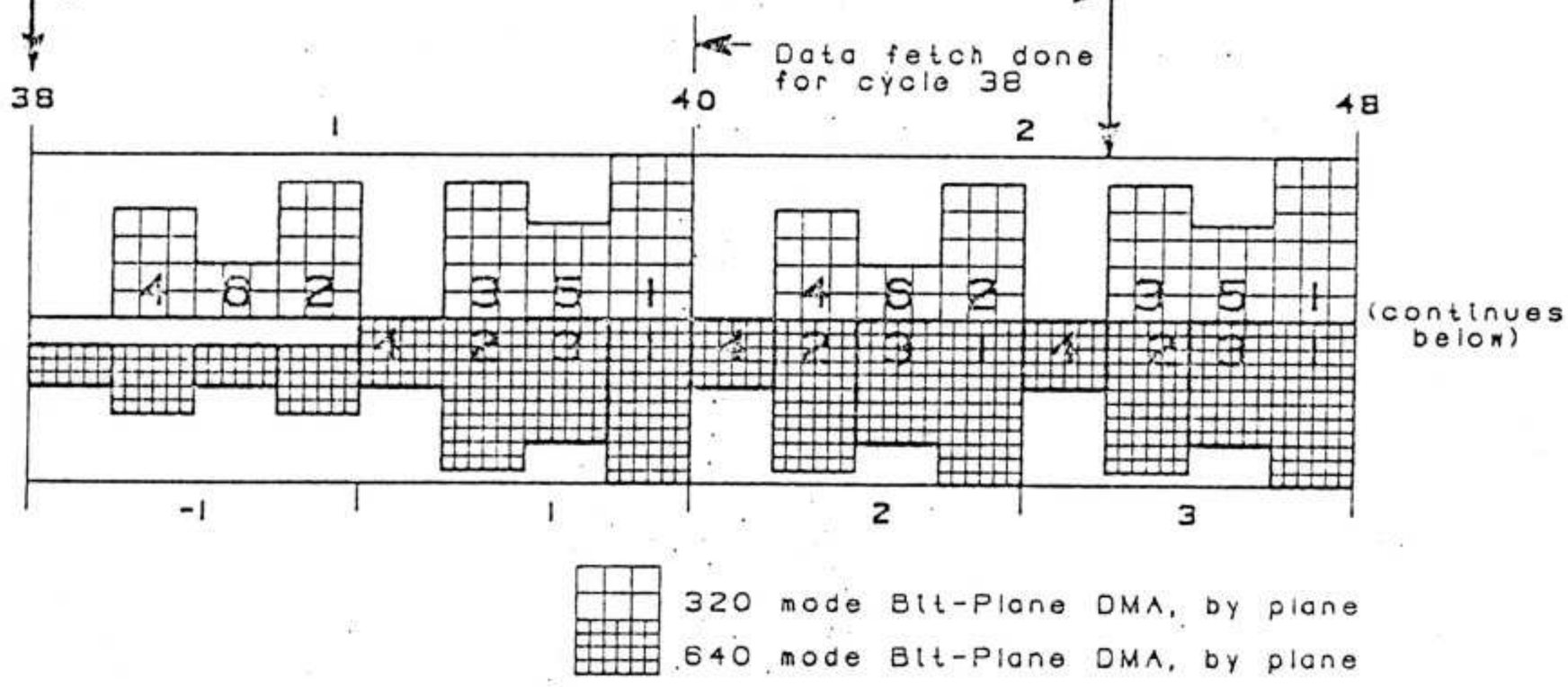
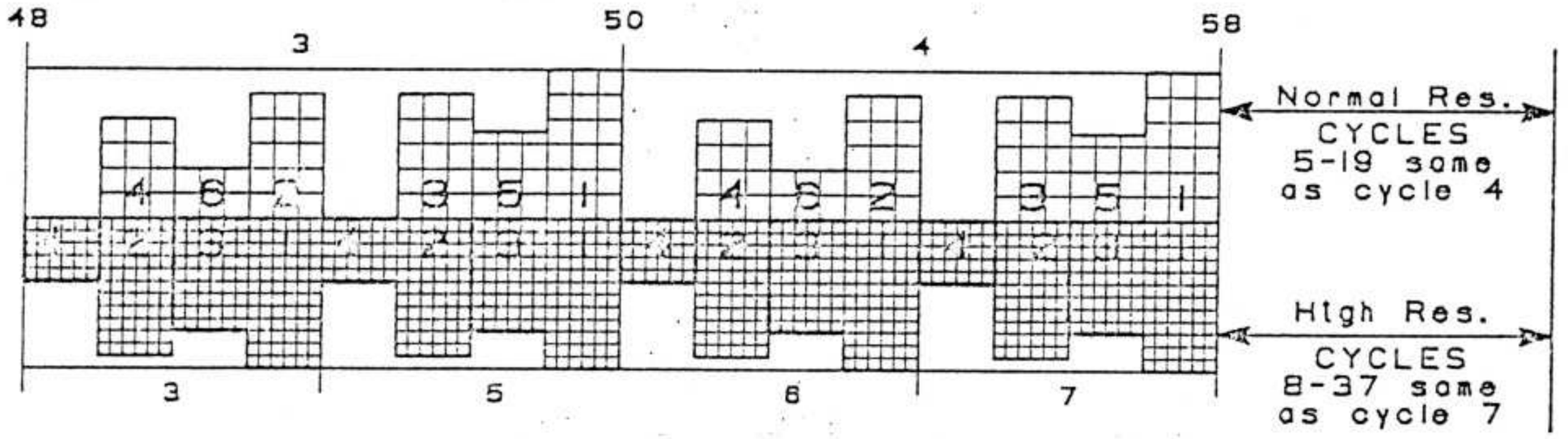
DMA Time Slot Allocation / Horizontal line (cont'd)

Data fetch start can only be specified at even multiples of 8 clocks. This is the clock position which should be specified for the normal width display. (20 word fetch for 320 pixel, 40 word fetch for 640 pixel width).

Five clocks must occur before the data which was fetched for a particular position can appear onscreen. For example, if data fetch start is specified as 38, it will not be available for display until clock number 45.





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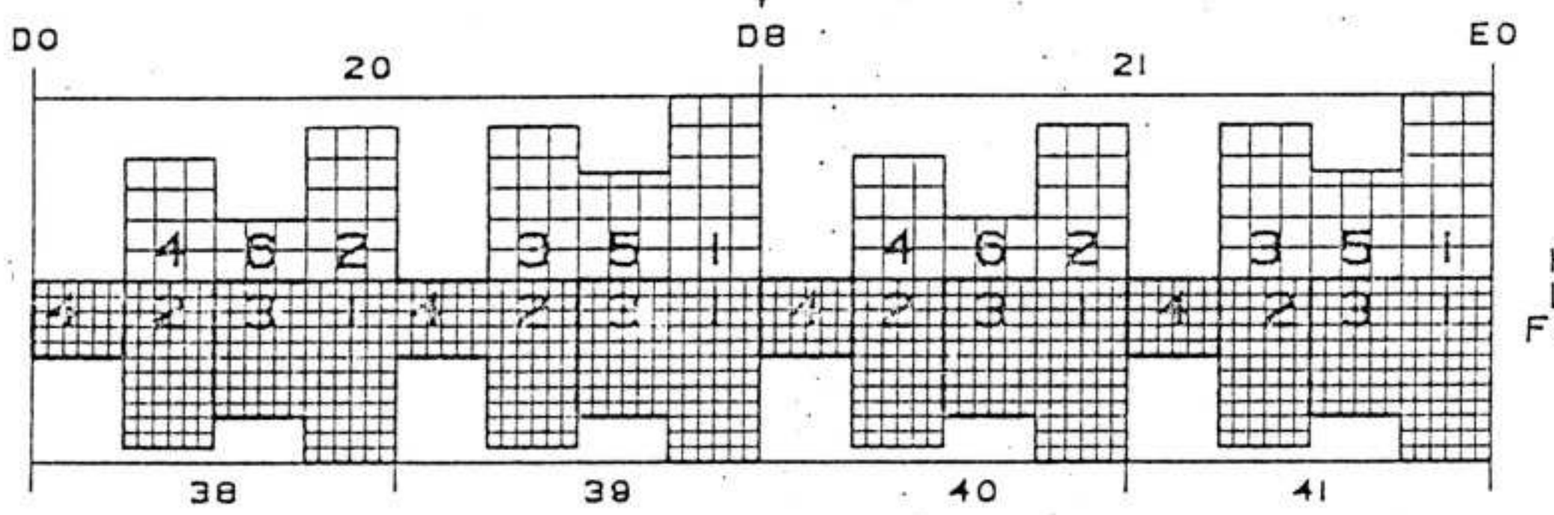
DMA Time Slot Allocation / Horizontal line (cont'd)

A hardware data-fetch stop has been installed at count D6 so as to prevent the bit-plane data-fetch from overrunning the time alloted for the memory refresh or disk DMA.



End of Horizontal Line Data Fetch Cycle

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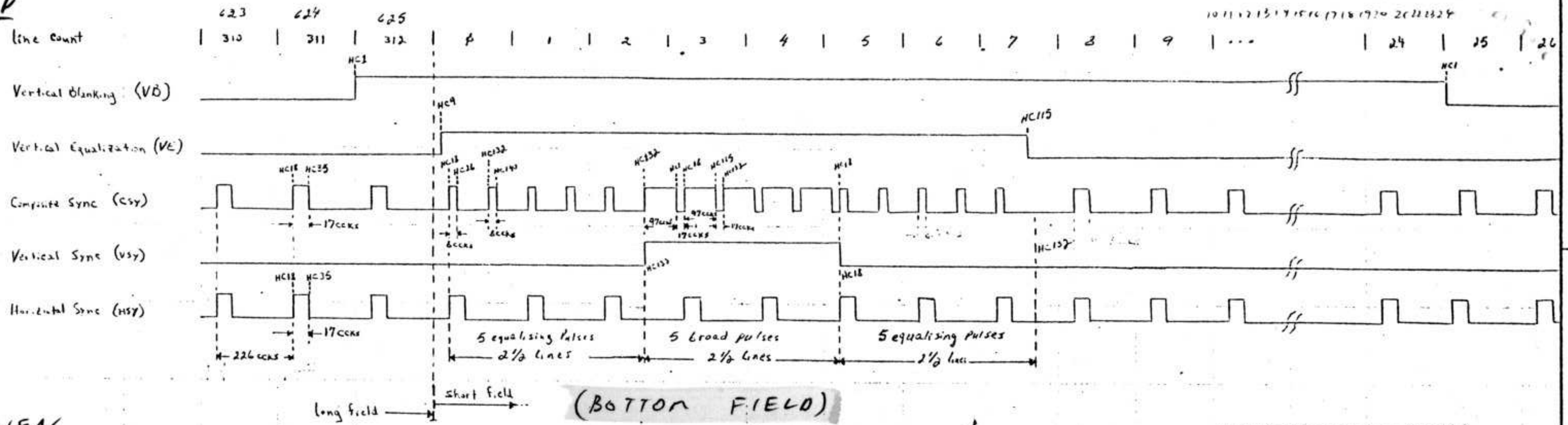
ODD

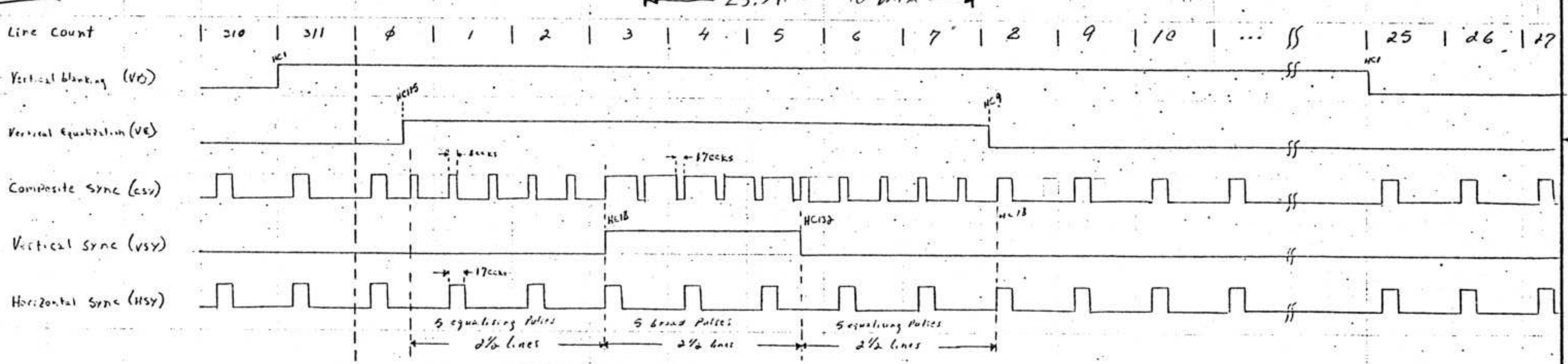


Long field — Short field

(BOTTOM FIELD)

23.5H — TO DATA

EVEN



SHORT FIELD — LONG FIELD

(TOP FIELD)

23H — TO DATA

HC = Horizontal Count

(color clock) 1 cclk = 283.75/2 = 3.5469 MHz

Line rate = 227 cclks = 64 µs → 15.625 KHz

(908 PIXELS/LINE @ 70.484184 nS/PIXEL)

Line Sync = 17 cclks = 4.79 µs

equalising Pulse = 8 cclks = 2.26 µs

broad pulse separation = 17 cclks = 4.79 µs

field blanking = 26 lines = 1.657 ms

field sync = 2½ lines = 159.3 µs

Interlace lines per picture = 625 = 312 + 313
ODD (SHORT) EVEN (LONG)

(NO SHORT/LONG LINE METHOD)

NON-INTERLACE MODE: EVEN FIELDS

APPENDIX B
PAL VIDEO SYNCHRONIZATION PULSES

UNLESS OTHERWISE SPECIFIED TOLERANCES ON: DECIMALS .X ± .XX ± .XXX ± ∠'s ±	DRAWN BY: KEN	DATE 6-10-87	commodore
	CHKD:		8371 - PAL FAT AGNUS 8378 - HR. FAT AGNUS PAL Video Synchronization Pulses
	ENGR: KEN		
	APPR:		
MATERIAL:	USED ON	NEXT ASSY	SIZE C 318071 REV B
FINISH:			SCALE SHEET 39 OF

CENTENNIAL BLUEPRINT NO1006

APPROVED VENDORS LIST

This page must be detached from the remainder of the drawing whenever this drawing is shown or transmitted to vendors.

COMMODORE PART NUMBER	VENDOR NAME	VENDOR PART NUMBER
318071-01	MOS	8371R1
318071-01	MOS	8371R2

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